04-10-00

Case Docket No. US 000099

THE COMMISSIONER OF PATENTS AND TRADEMARKS, Washington, D.C. 20231

Enclosed for filing is the patent application of Inventor:
TIRDAD SOWLATI and VICKRAM VATHULYA

FOR: INTERDIGITATED MULTILAYER CAPACITOR STRUCTURE FOR DEEP SUB-MICRON CMOS

ENCLOSED ARE:

[X] Appointment of Associates;
[X] Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;
[ ] Preliminary Amendment;
[X] Specification (12 Pages of Specification, Claims, & Abstract);
[X] Declaration and Power of Attorney:
(2 Pages of a [X]fully executed [ ]unsigned Declaration);
[X] Drawing (4 sheets of [X]informal [ ]formal sheets);
[ ] Certified copy of Application Serial No. ;
[X] Authorization Pursuant to 37 CFR §1.136(a)(3)
[ ] Other: ;
[X] Assignment to Philips Electronics North America Corporation.

FEE COMPUTATION

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - $690.00
Total Claims	11 - 20 =		X $18 =	
Independent Claims	1 - 3 =		X $78 =	
Multiple Dependent Claims, if any			$260 =	
TOTAL FILING FEE			=	$ 690.00

Please charge Deposit Account No. 14-1270 in the amount of the total filing fee indicated above, plus any deficiencies. The Commissioner is also hereby authorized to charge any other fees which may be required, except the issue fee, or credit any overpayment to Account No. 14-1270.

[ ]Amend the specification by inserting before the first line as a centered heading --Cross Reference to Related Applications--; and insert below that as a new paragraph --This is a continuation-in-part of application Serial No. , filed , which is herein incorporated by reference--.

CERTIFICATE OF EXPRESS MAILING

Express Mail Maling Label No. EL 335 550 545 US
Daae of Deposit April 7, 2000
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INTERDIGITATED MULTILAYER CAPACITOR STRUCTURE FOR DEEP SUB-MICRON CMOS

RELATED APPLICATIONS

Commonly-assigned, copending U.S. Patent Application, No. , entitled "Combined Transistor-Capacitor structure In Deep Sub-Micron CMOS For Power Amplifiers", filed , 2000.

Commonly-assigned, copending U.S. Patent Application, No. , entitled "Multilayer Pillar Array Capacitor Structure For Deep Sub-Micron CMOS", filed , 2000.

Commonly-assigned, copending U.S. Patent Application, No. , entitled "Multilayered Capacitor Structure With Alternately Connected Concentric Lines For Deep Sub-Micron CMOS", filed , 2000.

Commonly-assigned, copending U.S. Patent Application, No. , entitled "Multilayer Capacitor Structure Having An Array Of Concentric Ring-Shaped Plates For Deep Sub-Micron CMOS", filed , 2000.

FIELD OF THE INVENTION

This invention relates to capacitor structures in metal-oxide-semiconductors (MOS), and in particular, to an interdigitated multilayer (IM) capacitor structure for deep sub-micron complementary MOS (CMOS), which is formed by interconnecting conductive lines in multiple levels through vias to construct a parallel array of vertical capacitor plates, and interconnecting the plates to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

BACKGROUND OF THE INVENTION

Conventional capacitor structures for deep sub-micron CMOS are typically constructed with two flat parallel plates separated by a thin dielectric layer. The plates are formed by layers of conductive material, such as metal or polysilicon. The capacitor structure is usually isolated from the substrate by an underlying dielectric layer. To achieve high capacitance density in these devices, additional plates are provided. FIGS. 1A and 1B illustrate a representative conventional multi-parallel plate capacitor 10 in a deep sub-micron CMOS structure. The capacitor structure 10 includes a vertical stack of electrically conductive lines 12 separated by dielectric layers 13. The conductive lines 12 and dielectric layers 13 are constructed over a semiconductor substrate 11. The conductive lines 12 form the plates or electrodes of the capacitor 10. The plates 12 are electrically connected together in an alternating manner such that all the "A" plates are of a first polarity and all the "B" plates are of a second polarity, opposite to the first polarity.

A major limitation associated with parallel plate capacitor structures is that the minimum distance between the plates does not change as geometries in CMOS processes are scaled down. Hence, gains in capacitance density are not realized during such down scaling.

Various other capacitor structures with high capacitance densities, such as double polysilicon capacitors and gate-oxide capacitors, are known in the art. Double polysilicon capacitors, however, do not lend themselves to deep sub-micron CMOS processes. Gate-oxide capacitors are generally not used in deep sub-micron CMOS processes because they have large gate areas which cause yield and reliability issues, they generate capacitances which vary with voltage, and may experience high voltages that can breakdown the gate-oxide.

Trench capacitor structures for dynamic random access memories (DRAMs) have high capacitance densities. Such capacitors are formed by etching a trench in the substrate and filling

the trench with conductive and dielectric material to form a vertical capacitance structure. However, trench capacitors are costly to fabricated because they add etching and trench filling processes.

Interdigitated capacitor structures are used in microwave applications. These capacitors have closely placed, interdigitated conductive line structures which produce fringing and cross-over capacitances therebetween to achieve capacitance. However, the cross-over capacitance produced by interdigitated capacitors is limited to a single conductor level.

Accordingly, a need exists for an improved capacitor structure for deep sub-micron CMOS, which takes advantage of shrinking semiconductor process geometries and can be manufactured inexpensively.

SUMMARY OF THE INVENTION

A capacitor structure comprising a first level of electrically conductive parallel lines and at least a second level of electrically conductive parallel lines disposed over the lines in the first level, the lines of the first and second levels being arranged in vertical rows. A dielectric layer is disposed between the first and second levels of conductive lines. One or more vias connect the first and second level lines in each of the rows, thereby forming a parallel array of vertical capacitor plates. Electrically opposing nodes form the terminals of the capacitor. The parallel array of vertical capacitor plates are electrically connected to the nodes in an alternating manner so that the plates have alternating electrical polarities.

BRIEF DESCRIPTION OF THE DRAWINGS

The advantages, nature, and various additional features of the invention will appear more fully upon consideration of the illustrative embodiments now to be described in detail in connection with accompanying drawings wherein:

FIG. 1A is a top view of a conventional parallel plate capacitor structure in a deep sub-micron integrated circuit structure;

FIG. 1B is a cross-sectional view through line 1B-1B of FIG. 1A;

FIG. 2A is a top view of an interdigitated multilayer (IM) capacitor according to one embodiment of the invention in a deep sub-micron CMOS structure;

FIG. 2B is a perspective view of a section of the IM capacitor of FIG. 2A;

FIG. 2C is an end view of the IM capacitor section of FIG. 2B; and

FIG. 3 is an end view of a conventional interdigitated capacitor.

It should be understood that the drawings are for purposes of illustrating the concepts of the invention and are not to scale.

DETAILED DESCRIPTION OF THE INVENTION

FIGS. 2A-2C illustrate an interdigitated multilayer (IM) capacitor structure 20 according an embodiment of the invention for generating capacitance in deep sub-micron CMOS. The IM capacitor structure 20 is constructed over a substrate 21 of semiconductor material (FIGS. 2B and 2C)in a multiple conductor level process (four electrical conductor levels L1-L4 are depicted for illustrative purposes only). The first conductor level L1 includes a first parallel array of electrically conductive horizontal lines 22, the second conductor level L2 includes a second parallel array of electrically conductive horizontal lines 23, the third conductor level L3 includes

a third parallel array of electrically conductive horizontal lines 24, and the fourth conductor level L4 includes a fourth parallel array of electrically conductive horizontal lines 25. A first dielectric layer 26 fills the space between the substrate 21 and the first conductor level L1; a second dielectric layer 27 fills the space between the first and second conductor levels L1, L2 and the spaces between the lines 22 of the first conductor level L1; a third dielectric layer 28 fills the space between the second and third conductor levels L2, L3 and the spaces between the lines 23 of the second level L2; a fourth dielectric layer 29 fills the space between the third and fourth conductor levels L3, L4 and the spaces between the lines 24 of the third conductor level L3; and a fifth dielectric layer 34 fills the spaces between the lines 25 of the fourth conductor level L4.

The four levels L1-L4 of conductive lines 23-25 are aligned over each other in vertical in rows or stacks. The conductive lines 23-25 in each row are electrically interconnected through vertically extending electrically conductive vias 30-32 formed in the second, third, and fourth dielectric layers 27-29. The rows of conductive lines 23-25 and vias 30-32 form a parallel array of vertically extending plates 33 which form the electrodes of the capacitor structure 20. The vertical plates 33 are electrically interdigitated into "A" and "B" plates of opposite polarity by electrically connecting the top or bottom of the A plates to a first common node A and electrically connecting the top or bottom of the B plates to a second common node B (FIG. 2A). The first and second nodes A, B form the terminals of the IM capacitor structure 20.

The mechanism by which the IM capacitor structure 20 of the present invention generates capacitance can be best understood by first examining a conventional single level interdigitated capacitor structure 40 as shown in FIG. 3. The interdigitated capacitor structure 40 has a total capacitance C_{Total} which is the sum of all the cross-over capacitance C_c between the interdigitated conductive lines 41 and all the fringing capacitance C_f between the interdigitated

conductive lines 41. In the interdigitated capacitor structure 40, the fringing capacitance C_f is comparable in quantity to the cross-over capacitance C_c.

The IM capacitor structure 20 of the invention also has a total capacitance C_{Total} which is the sum of all the cross-over capacitance C_c between the interdigitated vertical plates 33 (the sum of the cross-over capacitance between adjacent conductive lines and the cross-over capacitance between adjacent vias) and all the fringing capacitance C_f between the interdigitated vertical plates 33. However, unlike the conventional interdigitated capacitor structure 40, the quantity of cross-over capacitance C_c increases with each additional conductor level in the IM capacitor structure 20 while the quantity of fringing capacitance C_f does not change. Hence, the fringing capacitance in the IM capacitor structure 20 contributes less to its total capacitance C_{Total}. As additional conductor levels are used in the IM capacitor structure 20, the quantity of cross-over capacitance C_c becomes a dominant factor in the capacitor's total capacitance C_{Total}, while the quantity of fringing capacitance C_f becomes much less significant.

In present state-of-the-art deep sub-micron CMOS technology, conductive line spacings of about 0.5 microns or less is common. Thus, the minimum distance between the vertical plates of the IM capacitor structure 20of the invention is typically equal to or less than about 0.5 microns. (The height of the plates is typically greater than about 5 microns when stacking four levels of conductive lines.) The sub-micron spacings between the vertical plates 33 of the IM capacitor structure 20 of the invention provide it with increased capacitance density as compared to what can be achieved using conventional parallel plate capacitor structures.

The improvement in capacitance density can be seen by comparing the capacitance of a conventional parallel plate capacitor, similar to the one shown in FIGS. 1A and 1B, constructed with five (5) plates and having dimensions of 15 microns x 39 microns, with a capacitor

constructed with 4 conductor levels according to the invention (FIG. 2A) and having dimensions of 14.9 microns x 39 microns. Both capacitors were constructed in a 0.25 micron CMOS process. The parallel plate capacitance between nodes A and B of the parallel plate capacitor was found to be 95 fF, compared to the cross-over capacitance between nodes A and B of the IM capacitor which was found to be 150 fF. Hence, the IM capacitor structure of the present invention provides an increase of about 60 percent in capacitance density.

As the geometries in semiconductor process technologies continue to shrink and scale down, the capacitance density of the IM capacitor structure 20 of the invention will advantageously increase. This is because the minimum width M_w of the conductive lines 22-25 (FIG. 2C), the dimensions of the vias 30-32, the minimum distance M_{dv} between the vias 30-32 in the same vertical plate (FIG. 2B), and the minimum distance M_d between vertical plates 33 (FIG. 2C) of the IM capacitor structure 20 of the invention will advantageously decrease. As a result, the cross-over capacitance C_c of the IM capacitor structure 20 will increase. Such capacitance increases are not possible in conventional multilayer parallel plate capacitor structures because the heights or thicknesses of the conductor and dielectric levels do not scale down. Hence, the distance between the plates will remain about 1 micron in conventional parallel plate capacitor structures.

The IM capacitor structure of the invention is typically manufactured in silicon using conventional deep sub-micron CMOS processing. The capacitor structure of the invention can also be manufactured in gallium arsenide or any other suitable semiconductor system using conventional deep sub-micron processing. Manufacturing in silicon using deep sub-micron CMOS processing, usually involves growing or depositing a first layer of silicon dioxide on a selected portion of the silicon semiconductor substrate to form the first dielectric layer. The

silicon dioxide layer has a thickness in the range of about one micron. A first layer of metal, such as aluminum, or highly conductive polysilicon, is deposited on the first dielectric layer of silicon dioxide and then defined into the conductive lines using well known masking and dry etching techniques to form the first conductor level. As mentioned above, the width and spacing of the conductive lines are set to the minimum dimensions of the process to enhance the capacitance of the structure, i.e., the lines and spacing between the lines are as narrow as possible.

A second layer of silicon dioxide is then grown or deposited over the conductive lines to form the second dielectric layer. The thickness of the second dielectric layer of silicon dioxide is in the range of about one micron. A plurality of holes, which extend down to the first conductor level are defined in the second dielectric layer of silicon dioxide and then filled with metal or polysilicon using conventional via fabrication techniques to form the vertically extending vias in the second dielectric layer. A second layer of metal, such as aluminum, or polysilicon, is deposited on the second dielectric layer of silicon dioxide and then defined into the conductive lines of the second conductor level. The remaining dielectric layers, vias, conductor levels, and conductive lines are fabricated in the same manner as described above.

One of ordinary skill in the art will recognized that specialized dielectric materials can be used in place of silicon dioxide (silicon systems) or silicon nitride (galium arsenide systems) to form the dielectric layers. For example a ferro-electric ceramic, such as PLZT (lanthanum-modified lead zirconate tantalate) can be used to form the dielectric layers. The use of PLZT layers greatly enhances capacitance as PLZT has a dielectric constant of approximately 4,700, in contrast to 3.9 for the dielectric constant of silicon dioxide.

The ordinary skill artisan will further recognize that the IM capacitor structure of the invention can be useful in many applications, such as RF, analog and digital applications. RF

circuit applications employ capacitors for matching. The larger the capacitance per unit area, the smaller the area and the lower the cost. In analog circuit applications, undesirable noise can often be reduced by using large capacitors (KT/C). In digital circuit applications, large decoupling capacitances are often very important and can be easily provided with the capacitor of the invention.

While the foregoing invention has been described with reference to the above embodiments, additional modifications and changes can be made without departing from the spirit of the invention. Accordingly, all such modifications and changes are considered to be within the scope of the appended claims.

CLAIMS

What is claimed is:

1. A capacitor comprising:

a first level of electrically conductive parallel lines;

at least a second level of electrically conductive parallel lines disposed over the lines in the first level, the lines of the first and second levels being arranged in vertical rows;

a dielectric layer disposed between the first and second levels of conductive lines;

at least one via connecting the lines in each of the rows, thereby forming a parallel array of vertical capacitor plates; and

electrically opposing nodes forming the terminals of the capacitor, the parallel array of vertical capacitor plates electrically connected to the opposing nodes in an alternating manner so that the plates have alternating electrical polarities.

2. The capacitor of claim 1, wherein the conductive lines comprise metal.

3. The capacitor of claim 1, wherein the conductive lines comprise polysilicon.

4. The capacitor of claim 1, wherein the dielectric layer comprises silicon dioxide.

5. The capacitor of claim 1, further comprising:

at least a third level of electrically conductive parallel lines disposed over the second level lines in manner which extends the rows vertically;

a second dielectric layer disposed between the second and third levels of conductive lines; and

at least one via connecting the second and third level lines in each of the rows so that the third level of lines vertically extends the parallel array of vertical capacitor plates.

6. The capacitor of claim 1, wherein the first and the at least second multiple levels of electrically conductive parallel lines comprise a plurality of electrically conductive parallel lines arranged in vertical rows, and the dielectric layer comprises a plurality of dielectric layers, each of the layers disposed between opposing levels of conductive lines.

7. The capacitor of claim 1, wherein the capacitor is constructed over a substrate.

8. The capacitor of claim 7, wherein the substrate is made from a semiconductor material.

9. The capacitor of claim 1, wherein the capacitor comprises a sub-micron MOS structure.

10. The capacitor of claim 1, wherein the capacitor comprises a sub-micron CMOS structure.

11. The capacitor of claim 1, wherein the capacitor comprises a sub-micron structure.

ABSTRACT OF THE DISCLOSURE

A capacitor structure having a first level of electrically conductive parallel lines and at least a second level of electrically conductive parallel lines disposed over the lines in the first level, the lines of the first and second levels being arranged in vertical rows. A dielectric layer is disposed between the first and second levels of conductive lines. One or more vias connect the first and second level lines in each of the rows, thereby forming a parallel array of vertical capacitor plates. Electrically opposing nodes form the terminals of the capacitor. The parallel array of vertical capacitor plates are electrically connected to the nodes in an alternating manner so that the plates have alternating electrical polarities.

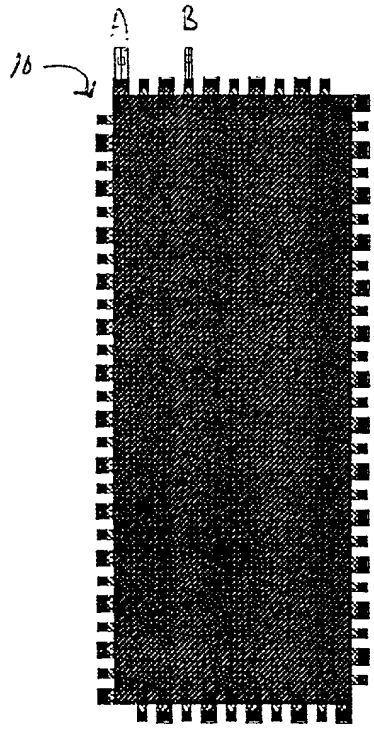


Fig. 1A
(Prior Art)

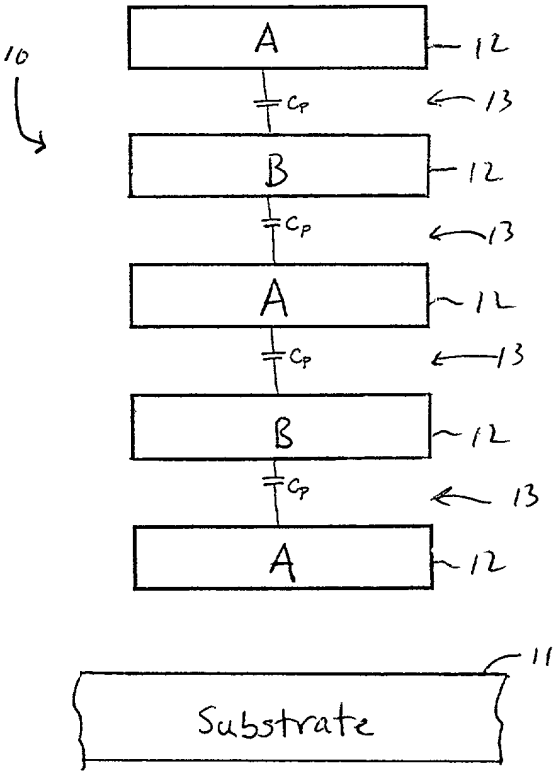


Fig. 1B
(Prior Art)

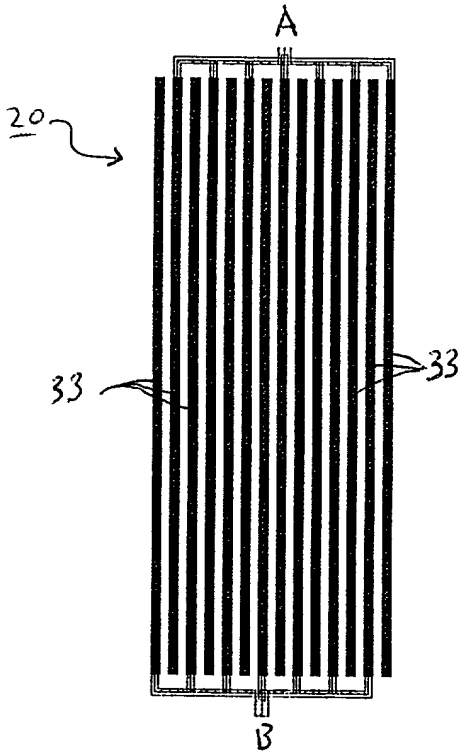
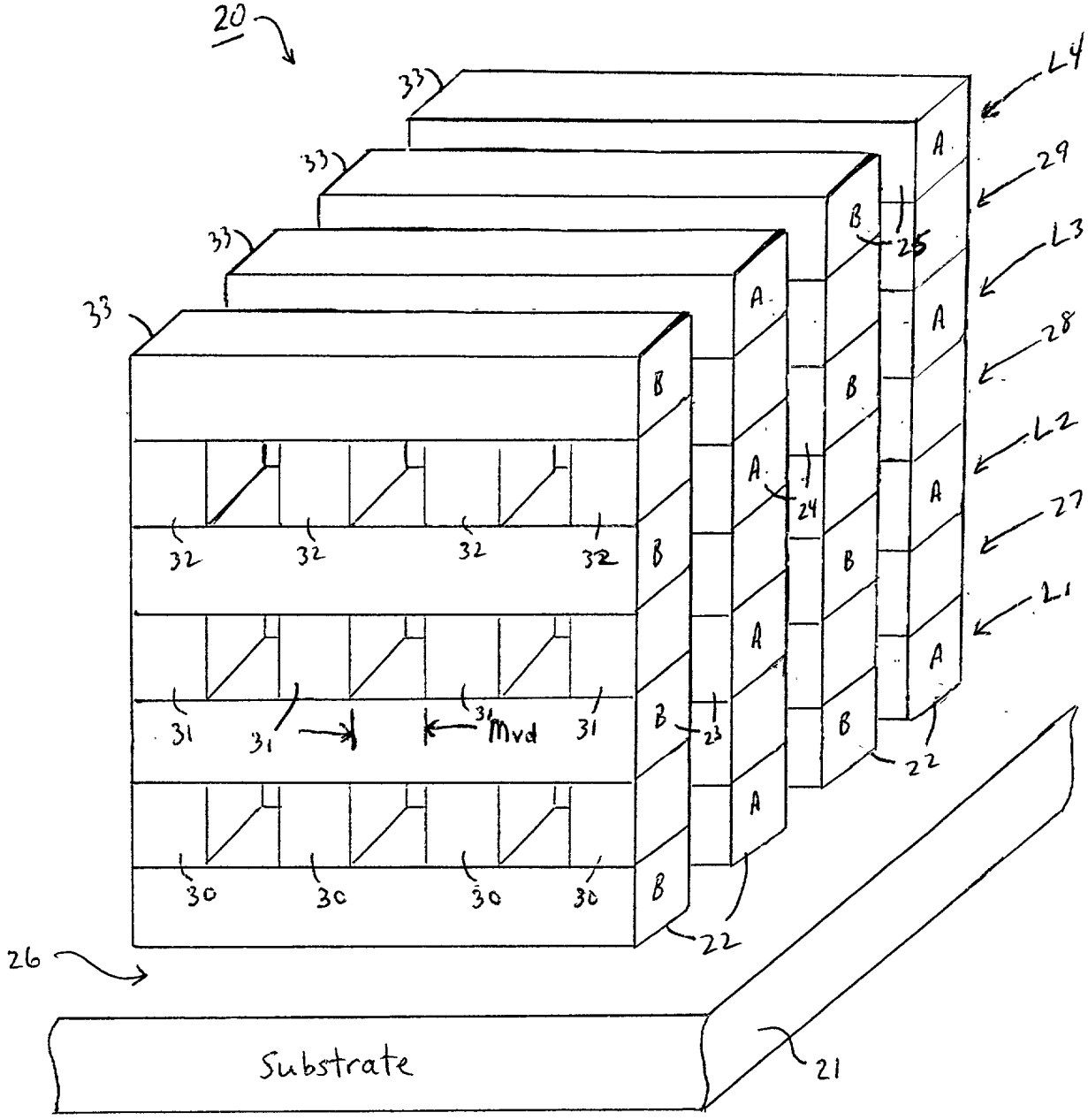


Fig. 2A


20
33
L4
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L3
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L2
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L1
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B
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Mvd
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Substrate
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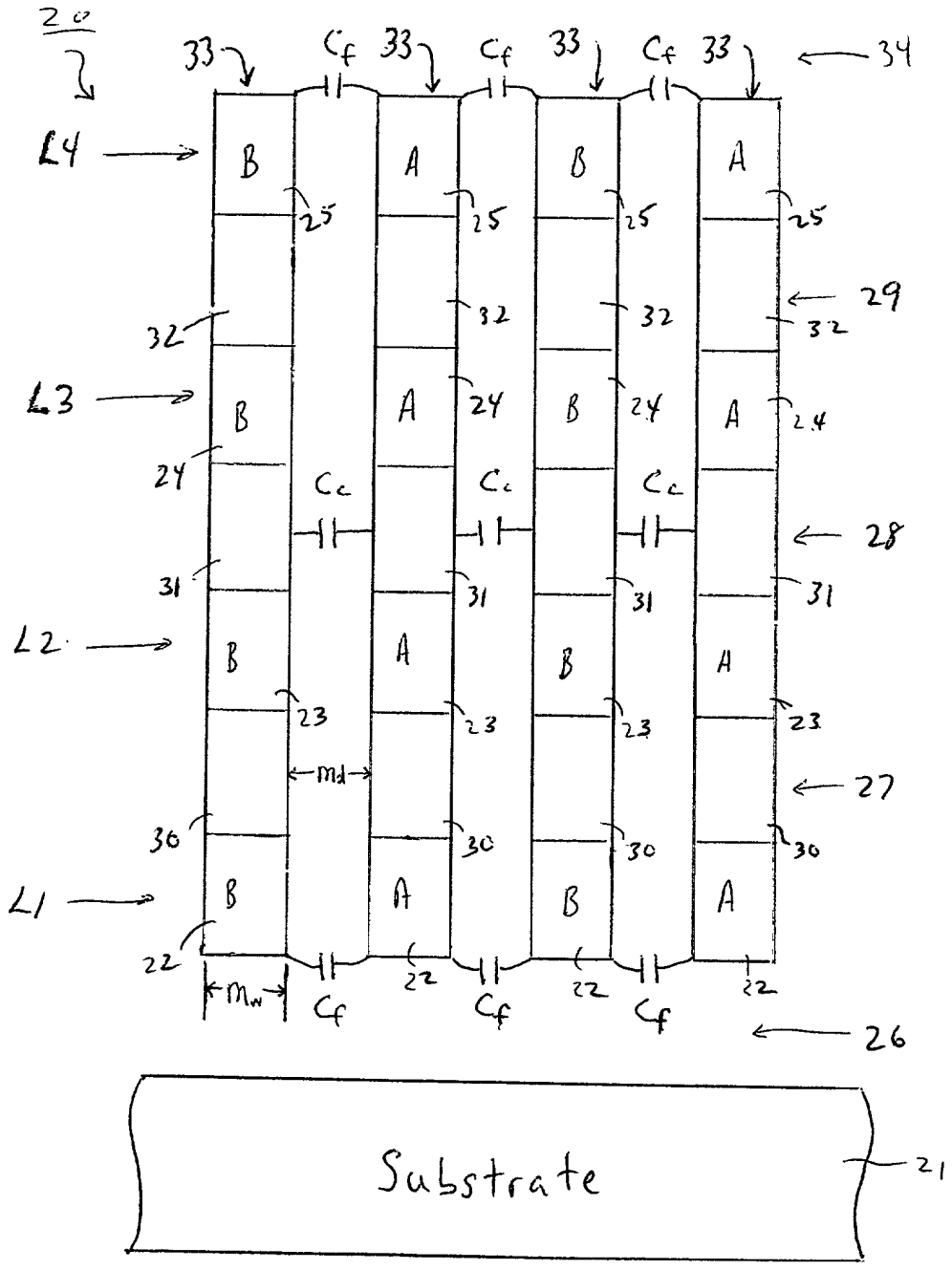
Fig. 2B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L1
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mw
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Substrate
21

Fig. 2C

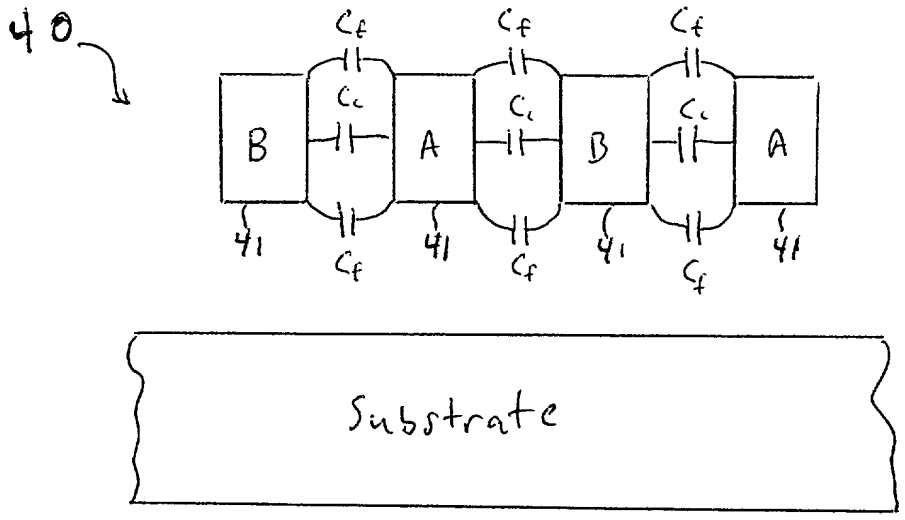

Fig 3 (Prior ART)

DECLARATION and POWER OF ATTORNEY

701052

Attorney's Docket No.
US 000099

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **INTERDIGITATED MULTILAYER CAPACITOR STRUCTURE FOR DEEP SUB-MICRON CMOS**

The specification of which (check one)

XX is attached hereto.

___ was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulation, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (DAY, MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application (s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Algy Tamoshunas, Reg. No. 27,677
Jack E. Haken, Reg. No. 26,902
Michael E. Marion, Reg. No. 32,266
Edward Blocker, Reg. No. 30,245

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Corporate Patent Counsel; U.S. Philips Corporation; 580 White Plains Road; Tarrytown, NY 10591	(name and telephone No.) John C. Fox (914) 333-9635

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Dated:		INVENTOR'S SIGNATURE:		
Full Name of Inventor	Last Name	FIRST NAME	Middle Name	
Residence & Citizenship	City	STATE OR FOREIGN COUNTRY	Country of Citizenship	
Post Office Address	Street	CITY	State or Country	Zip Code

Dated:		INVENTOR'S SIGNATURE:		
Full Name of Inventor	Last Name	FIRST NAME	Middle Name	
Residence & Citizenship	City	STATE OR FOREIGN COUNTRY	Country of Citizenship	
Post Office Address	Street	CITY	State or Country	Zip Code

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

TIRDAD SOWLATI ET AL

Atty. Docket

US 000099

Serial No.

Filed: CONCURRENTLY

INTERDIGITATED MULTILAYER CAPACITOR STRUCTURE FOR DEEP SUB-MICRON CMOS

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

The undersigned Attorney of Record hereby revokes all prior appointments (if any) of Associate Attorney(s) or Agent(s) in the above-captioned case and appoints:
John C. Fox (Registration No. 24,975)
c/o U.S. PHILIPS CORPORATION, Intellectual Property Department, 580 White Plains Road, Tarrytown, New York 10591, his Associate Attorney(s)/Agent(s) with all the usual powers to prosecute the above-identified application and any division or continuation thereof, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

Jack E. Haken, Reg. 26,902
Attorney of Record

Dated at Tarrytown, New York
April 6, 2000.

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